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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/528,730	03/22/2005	Oliver Brasse	2002P03695WOUS	8582

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Siemens Corporation
Intellectual Property Department
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EXAMINER	
ELAHEE, MD S	
ART UNIT	PAPER NUMBER
2614	
MAIL DATE	DELIVERY MODE
04/28/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/528,730	BRASSE ET AL.	
	Examiner	Art Unit	
	MD S. ELAHEE	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/22/2005,04/29/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statements (IDS's) submitted on March 22, 2005 and April 29, 2005 were received. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Claim Objections

2. Claim 27 is objected to because of the following informalities: regarding claim 27, the phrase "MOH (=Music on Hold)" in line 2 should apparently be "MOH (Music on Hold)". Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 12, 13, 24 and 27-31 are rejected under 35 U.S.C. 102(e) as being anticipated by McCormack et al. (U.S. Pub. No. 2002/0136384).

Regarding claims 12, 29 and 30, with respect to Figures 1-5, McCormack teaches a method for handling digital sound sequences in a telecommunications system having a CPU, a working memory for the CPU, and a switching network, the method comprising:

establishing connections to a telecommunication terminal via the switching network by the telecommunications system (fig.2,5);

McCormack further teaches outputting sound sequences via the switching network to the telecommunications terminal by the telecommunications system (page 3, paragraphs 0059, 0061-0062, page 4, paragraphs 0069-0071, 0073, 0076, 0078); and

McCormack further teaches using at least a part of the working memory to store the digital sound sequences (page 4, paragraph 0076).

Regarding claim 13, McCormack, as applied to claim 12, teaches that the CPU performs a data transfer of the digitally stored sound sequences between the working memory and switching network (page 1, paragraph 0002, page 3, paragraphs 0059, 0061, page 4, paragraphs 0069-0071, 0073, 0076, 0078).

Regarding claim 24, McCormack, as applied to claim 12, teaches that digitizing sound sequences and storing the digitized sound sequences in the working memory by the telecommunications system (page 3, paragraph 0059, page 4, paragraphs 0069-0071, 0076, 0078).

Regarding claim 27, McCormack, as applied to claim 12, teaches that the digital sound sequences are MOH (=Music on Hold), voice sequences, or signal tones (page 3, paragraph 0059, page 4, paragraphs 0069-0071, 0076, 0078).

Regarding claim 28, McCormack, as applied to claim 12, teaches program code and/or data of telecommunications subscribers being stored in the working memory (fig.7,8; page 3, paragraph 0059, page 4, paragraphs 0069-0071, 0076, 0078).

Regarding claim 31, McCormack, as applied to claim 30, teaches that the mechanisms for performing the method as claimed in claim 12 are program mechanisms and/or program modules (fig.7,8).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 14-23, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCormack et al. in view of Moran (U.S. Patent No. 4,370,743).

Regarding claims 14 and 15, McCormack, as applied to claims 12 and 13, teaches that data is transferred packet by packet (page 3, paragraphs 0059, 0061-0062, page 4, paragraphs 0069-0071, 0073, 0076, 0078).

However, McCormack does not specifically teach a time slot assigner (TSA) is used between the working memory and the switching to assign the digital sound sequences to programmed timeslots. Moran teaches a time slot assigner (TSA) is used between the working memory and the switching to assign the digital sound sequences to programmed timeslots (col.6, lines 1-22). Thus, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify McCormack to incorporate the feature of a time slot assigner (TSA) used between the working memory and the switching to assign the digital sound sequences to programmed timeslots in McCormack's invention as taught by Moran. The motivation for the modification is to do so in order to provide sound within a particular time.

Regarding claims 16 and 17, McCormack, as applied to claims 14 and 15, teaches supporting a packet-by-packet data transfer of the digital sound sequences (page 3, paragraphs 0059, 0061-0062, page 4, paragraphs 0069-0071, 0073, 0076, 0078).

However, McCormack does not specifically teach that a FIFO shift register is used in the time slot assigner (TSA). Moran teaches that a FIFO shift register is used in the time slot assigner (TSA) (ccol.5, lines 31-51, col.6, lines 1-22, col.8, line 61-col.9, line 18). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify McCormack to incorporate the feature of using a FIFO shift register in the time slot assigner (TSA) in McCormack's invention as taught by Moran. The motivation for the modification is to do so in order to provide a better service to a call.

Regarding claims 18 and 20, McCormack, as applied to claims 12 and 13, teaches the CPU to perform the transfer of the digital sound sequences (page 3, paragraphs 0059, 0061-0062, page 4, paragraphs 0069-0071, 0073, 0076, 0078).

However, McCormack does not specifically teach in order to unload the CPU a microcontroller is used between the working memory and a time slot assigner (TSA), wherein the microcontroller is initialized by the CPU. Moran teaches in order to unload the CPU a

microcontroller is used between the working memory and a time slot assigner (TSA), wherein the microcontroller is initialized by the CPU (fig.1; col.5, lines 18-30). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify McCormack to incorporate the feature of a time slot assigner (TSA) used between the working memory and the switching to assign the digital sound sequences to programmed timeslots in McCormack's invention as taught by Moran. The motivation for the modification is to do so in order to provide fast processing service by a CPU.

Regarding claim 19, McCormack in view of Moran, as applied to claim 18, does not specifically teach that the microcontroller is a Direct Memory Access (DMA) controller. Examiner notes that the microcontroller as a Direct Memory Access (DMA) controller is well known in the art. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify McCormack in view of Moran to incorporate the feature of the microcontroller as a Direct Memory Access (DMA) controller in McCormack's invention in view of Moran's invention in order to provide quick data retrieval control from a memory.

Regarding claim 21, McCormack, as applied to claim 21, teaches that the CPU requests the microcontroller to set the start address of the digital sound sequences in the working memory in order to play back the digital sound sequences (page 3, paragraphs 0059, 0061-0062, page 4, paragraphs 0069-0071, 0073, 0076, 0078).

However, McCormack does not specifically teach that the CPU requests the microcontroller to set the start address of the digital sound sequences in the working memory and

to set the destination address in the FIFO shift register of the time slot assigner (TSA). Moran teaches that the CPU requests the microcontroller to set the start address of the digital sound sequences in the working memory and to set the destination address in the FIFO shift register of the time slot assigner (TSA) (fig.1; col.5, lines 31-68). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify McCormack to incorporate the feature of the CPU requesting the microcontroller to set the start address of the digital sound sequences in the working memory and to set the destination address in the FIFO shift register of the time slot assigner (TSA) in McCormack's invention as taught by Moran. The motivation for the modification is to do so in order to properly play back sound/audio message to a user.

Claims 22 and 23 are rejected for the same reasons as discussed above with respect to claim 21. Furthermore, McCormack, as applied to claims 18 and 21, teaches the CPU requests to set the destination address in the working memory for recording sound sequences (page 3, paragraphs 0059, 0061-0062, page 4, paragraphs 0069-0071, 0073, 0076, 0078).

Regarding claim 25, McCormack, as applied to claim 12, does not specifically teach that at a certain filling level of the FIFO shift register, the time slot assigner (TSA) requests the CPU by an interrupt command to start or to stop a new data transfer. Moran teaches that at a certain filling level of the FIFO shift register, the time slot assigner (TSA) requests the CPU by an interrupt command to start or to stop a new data transfer (fig.1; col.5, lines 31-68). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to

modify McCormack to incorporate the feature of the time slot assigner (TSA) requesting the CPU by an interrupt command to start or to stop a new data transfer at a certain filling level of the FIFO shift register in McCormack's invention as taught by Moran. The motivation for the modification is to do so in order to stop recording data in memory when the memory is full.

Regarding claim 26, McCormack, as applied to claim 12 , does not specifically teach that in order to unload the CPU a CPU with integrated Peripheral Exchange Control (PECC) transfer feature is used between the working memory and a time slot assigner (TSA). Moran teaches that in order to unload the CPU a CPU with integrated Peripheral Exchange Control (PECC) transfer feature is used between the working memory and a time slot assigner (TSA) (fig.1; col.5, line 18-col.6, line 22). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify McCormack to incorporate the feature of using a CPU with integrated Peripheral Exchange Control (PECC) transfer feature between the working memory and a time slot assigner (TSA) in order to unload the CPU in McCormack's invention as taught by Moran. The motivation for the modification is to do so in order to provide fast data processing service by a CPU.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MD S. ELAHEE whose telephone number is (571)272-7536. The examiner can normally be reached on Mon to Fri from 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fan Tsang can be reached on (571) 272-7547. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/MD S ELAHEE/
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